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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,771	09/22/2003	Yusuke Igarashi	14225-024001 / F1030479US	1356

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,771	IGARASHI ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-18* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *083104*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the rear surface". There is insufficient antecedent basis for this limitation in the claim.

Claims 2-18 are indefinite because they depend on claim 1

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6, 8, 10-18 rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima et al (US 6,828,221) in view of Asahi et al (US 2002/0135058)

Iijima discloses a method for manufacturing wiring circuit substrate. The method comprises the steps of:

preparing a laminated plate by laminating a first conductive film 21 and a second conductive film 23 via a third conductive film 22 (col 24, lines 10-14)

forming a first conductive wiring layer by etching said first conductive 21 film into a desirable pattern (col 24, lines 31-35)

selectively removing said third conductive 22 film by use of said first conductive wiring layer as a mask (col 24, lines 51-55)

laminating an insulating sheet where a first insulating layer 27 has been fitted to a fourth conductive film 29 so that said first insulating layer 27 covers front-surface portions of the second conductive film exposed by removing said third conductive film, said first conductive wiring layer, and end fades of the third conductive film (col 25, lines 1-20; fig. 2B)

forming a second conductive wiring layer by etching said fourth conductive film into a desirable pattern (col 25, lines 24-26)

forming multilayer connecting means 26 and thus electrically connecting said first conductive wiring layer with said second conductive wiring layer (col 25, lines 25-30; fig. 2D)

covering the second conductive wiring layer with a second insulating layer (fig. 4B)

partially removing the second insulating layer to expose the second conductive wiring (fig. 4a)

fitting LSI chip/semiconductor elements onto the second insulating layer to electrically connect the chip/semiconductor elements with the second wiring layer (col 31, lines 13-16)

removing the second conductive film 22 to expose the third conductive film on a rear surface (col 27, lines 20-25; fig. 3F)

Unlike the instant claimed invention as per claim 1, Iijima fails to disclose a step of covering the semiconductor element with a sealing resin layer

Asahi discloses a method for manufacturing a module comprises the step of covering the semiconductor element with a sealing resin layer (col 4, paragraph 0059)

One skilled in the art at the time the invention was made would have found it obvious to modify Iijima method by adding the step of covering the semiconductor element with a sealing resin layer as per Asahi because Asahi discloses that semiconductor elements may be embedded in a manner such that semiconductor elements is sealed with a sealing resin for connecting with the wiring pattern (col 4, paragraph 0059)

Regarding claim 2, fig. 1D of Iijima shows that the etching is performed up to the third conductive line 22, fig. 1D)

Regarding claims 3, 6, Iijima discloses using wet etching to etch layer 21/ first conductive film and layer 22/third conductive film (col 24, lines 45-48)

Regarding claim 8, Iijima discloses that the entire layer 23/second conductive film is etched (fig. 2D)

Regarding claim 10, Iijima discloses forming an insulating sheet using a heating roller (col 24, lines 59-60), the insulating layer may be formed of resin material (col 40, lines 45-46)

Regarding claim 11, Iijima discloses that the first and second conductive 21 and 23 are copper (col 24, lines 10-15)

Regarding claims 12-13, 15, Iijima discloses using a base to form the conductive layer by plating (col 24, lines 15-20, using a heating roller to press-bond the insulating later (col 24, lines 59-60)

Regarding claim 14, fig. 8C shows that the first conductive film and the wiring circuit are connected

Regarding claim 16, Iijima discloses using laser to form through hole through the insulating layer (col 57, lines 21-26)

Regarding claim 17, Iijima discloses using resist film as mask/lithography method (col 28, lines 24-25)

Regarding claim 18, Iijima discloses forming through holes trough the insulating layer to connect the wiring layers (fig. 46D)

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima et al (US 6,828,221) in view of Asahi et al (US 2002/0135058) and further in view of Hayashi et al (US 6,143,116)

Iijima as modified by Asahi has been described above. Unlike the instant claimed invention as per claim 4, Iijima and Asahi fail to disclose etching the conductive layer using a solution contains ferric chloride or cupric chloride

Hayashi discloses a method for producing wiring board comprise the step of etching the conductive layer using a solution contains ferric chloride or cupric chloride (col, lines 10-11)

One skilled in the art at the time the invention was made would have found it obvious to modify Iijima and Asahi by etching the conductive layer using a solution contains ferric chloride or cupric chloride to remove the non-patterned portion to form a wiring circuit layer as taught by Hayashi (col 14, lines 10-12)

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima et al (US 6,828,221) in view of Asahi et al (US 2002/0135058) and further in view of Yamamoto et al (US 2002/0079133)

Iijima as modified by Asahi has been described above. Unlike the instant claimed invention as per claim 5, Iijima and Asahi fail to disclose removing the third conductive layer by electrolytic peeling

Yamamoto discloses a method for producing wiring board comprises the step of removing the third conductive layer by electrolytic peeling (col 1, paragraph 0006)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Iijima and Asahi by removing the third conductive layer by electrolytic peeling as per Yamamoto because according to Yamamoto, the metal/copper foil is removed by peeling (col 1, paragraph 0004)

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima et al (US 6,828,221) in view of Asahi et al (US 2002/0135058) and further in view of Kishida et al (US 5,299,789)

Iijima as modified by Asahi has been described above. Unlike the instant claimed invention as per claim 7, Iijima and Asahi fail to disclose etching the conductive layer using an iodine-based solution

Kishida discloses a method for forming conductor layer comprises the step of etching the conductive layer using an iodine-based solution (col 9, lines 6-8)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Iijima and Asahi by etching the conductive layer using an iodine-based solution as per Kishida because Kishida discloses that a mixture solution of iodine which is used for successively etching the copper layer (col 9, lines 5-8)

Allowable Subject Matter

7. Claim 9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
September 14, 2005